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| Faculty of Engineering and Computing  Department of Aerospace, Electronic and Electrical Engineering  6040CEM Individual Project Realization  **Project Logbook**  Software-based Control System and Validation Model for Voltage Source Inverter  Author: Wong Jun Jie  Student ID (CU): 11843544  Supervisor: Mr. Chai Yoon Yik  Submitted in partial fulfillment of the requirements of the Degree of Bachelor of Electrical and Electronic Engineering  **Session: Apr 2024**  **Project Log Sheet 1 (Session Jan 2024)**  **Week Number: Week 1 Start Date – End Date: 8 Jan – 12 Jan 2024**  **Student Name: WONG JUN JIE Supervisor Name: Chai Yoon Yik**  **Project Title:** Software-based Control System and Validation Model for Voltage Source Inverter  **Activity:**  Initiate Design in MATLAB Simulink. Getting research paper to know about the design procedure of the environment.  **Goal(s):**  To Initiate the foundation of the development of the Single-Phase Inverter Model.  **Previous Progress**: NA  **Current Progress**: Determining Topology, Setting up Simulink Environment  **Testing, Result and Finding:** SRF Current Control will be used. Currently several papers have been studied to confirm the design flow for the Inverter. Below shows the overview of a Voltage Source GCI (Grid Connected Inverter)    **Future Plan:**  Obtaining the Output Filter Value. Obtained the circuit’s frequency response curve.  **Supervisor’s remark:**    Note: Put NA if not applicable.  **Project Log Sheet 2 (Session Jan 2024)**  **Week Number: Week 2 Start Date – End Date: 15 Jan- 19 Jan**  **Student Name: Wong Jun Jie Supervisor Name: Chai Yoon Yik**  **Project Title:**  Software-based Control System and Validation Model for Voltage Source Inverter  **Activity:**  Design Output LCL Filter with damping resistor. Forming the Ideal Grid as a testing environment  **Goal(s):**  To Initiate the foundation of the development of the Single-Phase Inverter Model.  **Previous Progress**:  Initiate Design in MATLAB Simulink. Getting research paper to know about the design procedure of the environment.  **Current Progress**:  Done Obtaining the Output Filter Value. Obtained the circuit’s frequency response curve.  **Testing, Result and Finding:** The calculated LCL filter value had been determined using formula from a paper. Below shows the value and the frequency response of such filter.  **Future Plan:**. Implementing Bridge Inverter into the system.    **Supervisor’s remark:**  *Note: Put NA if not applicable.*  **Project Log Sheet 3 (Session Jan 2024)**  **Week Number: Week 3 Start Date – End Date: 22 Jan – 26 Jan 2024**  **Student Name: Wong Jun Jie Supervisor Name: Chai Yoon Yik**  **Project Title:** Software-based Control System and Validation Model for Voltage Source Inverter  **Activity:**  Designing the output Bridge modulator and Reference Signal. Setting up the Park-Clarke Transformation.  **Goal(s):**  To Initiate the foundation of the development of the Single-Phase Inverter Model.  **Previous Progress**:  Design Output LCL Filter with damping resistor. Forming the Ideal Grid as a testing environment  **Current Progress**:  Designing the SRF Block with Voltage and Current Reference. Need to implement current control into the system with the Reference Current Generation.  **Testing, Result and Finding:** PWM Modulator Block had been used for this case for ease of development and allowing for future C++ Code Export from MATLAB Simulink. As the project is more focused on the implementation,    **Future Plan:**. Implement a Ideal Grid System to Provide a Testing Ground with a Load    **Supervisor’s remark:**  *Note: Put NA if not applicable.* |
| **Project Log Sheet 4 (Session Jan 2024)**  **Week Number: Week 4 Start Date – End Date: 5 Feb – 9 Feb 2024**  **Student Name: Wong Jun Jie Supervisor Name: Chai Yoon Yik**  **Project Title:** Software-based Control System and Validation Model for Voltage Source Inverter  **Activity:**  Implement a Ideal Grid With Load Conditions for the Grid Connect VSI. Implement Several Sensors to obtain the value from the model.  **Goal(s):**  Implement a Ideal grid to test and validate a control systems.  **Previous Progress**:  Designing the SRF Block with Voltage and Current Reference. Need to implement current control into the system with the Reference Current Generation.  **Current Progress**: Implemented a Single-Phase Ideal Grid (240Vrms @50Hz). A 5kW load is connected to the grid to act as a load to the system. A Switch with snubber is implemented to allow smoother transition when connecting to the grid.  **Testing, Result and Finding:** To allow for better transition when connecting to the grid, a logic is required to control the relay.    **Future Plan:**.    **Supervisor’s remark:**  *Note: Put NA if not applicable.*  **Project Log Sheet 5 (Session Jan 2024)**  **Week Number: Week 5 Start Date – End Date: 12 Feb – 16Feb 2024**  **Student Name: Wong Jun Jie Supervisor Name: Chai Yoon Yik**  **Project Title:** Software-based Control System and Validation Model for Voltage Source Inverter  **Activity:**  Implement PI Current Controller into the systems.  **Goal(s):**  Implement PI Current Controller to control the injected power.  **Previous Progress**: Implemented a Single-Phase Ideal Grid (240Vrms @50Hz). A 5kW load is connected to the grid to act as a load to the system. A Switch with snubber is implemented to allow smoother transition when connecting to the grid.  **Current Progress**:  Implemented PI Current Controller into the system with a dq0 to abc reference converter. Currently the input reference is set to 1 for testing.  **Testing, Result and Finding:** The system equation can be visualized using the equation below. As we also need to regulate our Vd of the system, we also need to put in the information as shown as below.    **Future Plan:**.    **Supervisor’s remark:**  *Note: Put NA if not applicable.*  **Project Log Sheet 6 (Session Jan 2024)**  **Week Number: Week 6 Start Date – End Date: 1Feb -23 Feb 2024**  **Student Name: Wong Jun Jie Supervisor Name: Chai Yoon Yik**  **Project Title:** Software-based Control System and Validation Model for Voltage Source Inverter  **Activity:** Develop a current reference for direct current and quadrupole current reference for the PI controoler  **Goal(s): Control the injected power using the current reference.**  **Previous Progress**: Implemented PI Current Controller into the system with a dq0 to abc reference converter. Currently the input reference is set to 1 for testing.  **Current Progress**: Developing Functions to generate references.  **Testing, Result and Finding:** The reference can be obtained using equation below in such single-phase system.    **Future Plan:** Successfully Injecting Power into systems.  **Supervisor’s remark:**  *Note: Put NA if not applicable.*  **Project Log Sheet 7 (Session Jan 2024)**  **Week Number: Week 7 Start Date – End Date: 26 Feb – 4Mar 2024**  **Student Name: Wong Jun Jie Supervisor Name: Chai Yoon Yik**  **Project Title:** Software-based Control System and Validation Model for Voltage Source Inverter  **Activity: Develop a current reference for direct current and quadrupole current reference for PI Controller**`  **Goal(s): Control the injected power using the current reference.**  **Previous Progress**: Developing Functions to generate references.  **Current Progress**: Developing Reference Generation for DC Link Voltage Regulation  **Testing, Result and Finding:**  Reference Generation requires integration of the input and output DC Link Power to regulate the voltage. Such trapezoid method is develop for such application.    **Future Plan:**. Validating Output Power with the reference.  **Supervisor’s remark:**  *Note: Put NA if not applicable.*  **Project Log Sheet 8 (Session Apr 2024)**  **Week Number: Week 8 Start Date – End Date: 1 Apr – 5 Apr 2024**  **Student Name: Wong Jun Jie Supervisor Name: Chai Yoon Yik**  **Project Title:** Software-based Control System and Validation Model for Voltage Source Inverter  **Activity:** Validating Output Power with the reference.  **Goal(s): Validate the injected power with the reference.**  **Previous Progress**: Developed Power reference Generation. Pending Validation for the system performance.  **Current Progress**: Validating System Performance. Checking Output System Development  **Testing, Result and Finding:**  The Current Reference and the output power is almost identical. The transient happens as the injection point causes ripple to the system.    **Future Plan:**. Implementing a Injection Point Detection Logic to reduce the Transient.    **Supervisor’s remark:**  *Note: Put NA if not applicable.*  **Project Log Sheet 9 (Session Apr 2024)**  **Week Number: Week 9 Start Date – End Date: 8 Par -12 Apr 2024**  **Student Name: Wong Jun Jie Supervisor Name: Chai Yoon Yik**  **Project Title:** Software-based Control System and Validation Model for Voltage Source Inverter  **Activity:** Controlling the Injection Point of the Power  **Goal(s): Validate and control the point of injected power with the reference**  **Previous Progress**: Implementing a Injection Point Detection Logic to reduce the Transient.  **Current Progress**: Implementing an Injection Point Logic to reduce the transient.  **Testing, Result and Finding:** Injection Point Logic is implemented. From the waveform it shows that the injected current is inducing less transients.      **Future Plan:** Developing a DDSRF control for 3Phase Imbalanced Load Systems    **Supervisor’s remark:**  *Note: Put NA if not applicable.*  **Project Log Sheet 10 (Session Apr 2024)**  **Week Number: Week 10 Start Date – End Date: 15 Apr – 19 Apr 2024**  **Student Name: Wong Jun Jie Supervisor Name: Chai Yoon Yik**  **Project Title:** Software-based Control System and Validation Model for Voltage Source Inverter  **Activity:** DDSRF Control Loop Design  **Goal(s): Develop a DDSRF based control loop**  **Previous Progress**: NA  **Current Progress**: Initializing Design. Finding solution for Negative Sequence Extraction from the grid.  **Testing, Result and Finding:** As the DDSRF consists of a Negative Sequence Control and Decoupling network, further development is required in this case. Below is the controller which is designed to do control positive and negative sequence.      **Future Plan:**. Develop Power Reference Generation for such DDSRF Control systems.    **Supervisor’s remark:**  *Note: Put NA if not applicable.*  **Project Log Sheet 11 (Session Apr 2024)**  **Week Number: Week 11 Start Date – End Date: 22 Apr – 26 Apr 2024**  **Student Name: Wong Jun Jie Supervisor Name: Chai Yoon Yik**  **Project Title:** Software-based Control System and Validation Model for Voltage Source Inverter  **Activity:** DDSRF Power Control Loop Design  **Goal(s): Develop a DDSRF based control loop.**  **Previous Progress**: : Initializing Design. Finding solution for Negative Sequence Extraction from the grid.  **Current Progress** Develop Power Reference Generation for such DDSRF Control systems.  **Testing, Result and Finding:** As the DDSRF control is very different from the SRF Control. A special method of generating references is important. A specialized Reference Generation is designed to do provide positive and negative sequence reference to the control loop.      **Future Plan:**. Designing 3Phase 4Leg Modulation System, Testing the Circuit    **Supervisor’s remark:**  *Note: Put NA if not applicable.*  **Project Log Sheet 12 (Session Apr 2024)**  **Week Number: Week 12 Start Date – End Date: 29Apr – 3 May 2024**  **Student Name: Wong Jun Jie Supervisor Name: Chai Yoon Yik**  **Project Title:** Software-based Control System and Validation Model for Voltage Source Inverter  **Activity:** Validating Output Power with the reference.  **Goal(s): Develop a DDSRF based control loop**  **Previous Progress**: Develop Power Reference Generation for such DDSRF Control systems.  **Current Progress**: Designing 3Phase 4Leg Modulation System to allow Testing and validation of the Circuit  **Testing, Result and Finding:** 4 Leg Inverter require special modulation that as the 4th bridge is used to form a neutral in a 3 phase 4 wire connection. Currently we are designing a modulator and to use with such connection. This case we are trying to develop a OMIPWM to obtain the Neutral PWM Signal from our ABC reference.      **Future Plan:**. Finalizing development as it had reached the end of the development. Gathering data for single phase system to prepare for presentation .    **Supervisor’s remark:**  *Note: Put NA if not applicable.*  **Project Log Sheet 13 (Session Apr 2024)**  **Week Number: Week 13 Start Date – End Date: 6 May – 10 May 2024**  **Student Name: Wong Jun Jie Supervisor Name: Chai Yoon Yik**  **Project Title:** Software-based Control System and Validation Model for Voltage Source Inverter  **Activity:** Finalizing development as it had reached the end of the development. Gathering data for single phase system to prepare for presentation.  **Goal(s): Finalizing the Overall System Design**  **Previous Progress**: Designing 3Phase 4Leg Modulation System to allow Testing and validation of the Circuit  **Current Progress**: Setting up the Scopes to capture the signal on the SRF Single Phase System. Three Phase System development will be halted as it is not included in the project objective.  **Testing, Result and Finding:** Several scopes are required to obtain all the information of the system. THD% is obtained by Using the FFT analyzer in PowreGUI.  A screenshot of a computer screen  Description automatically generated  **Future Plan:**.NA    **Supervisor’s remark:**  *Note: Put NA if not applicable.* |